

ABSTRACT

Pipelined analog to digital conversion systems are provided having cascaded multi-bit successive approximation register subconverter stages.

- 5 Capacitor arrays are provided in the subconverter stages, where switching logic selectively couples the capacitors to operate in sample, conversion, and residue amplification modes for generating multi-bit subconverter digital outputs and analog subconverter residue outputs. In one implementation, the capacitors are switched according to a thermometer code to reduce differential converter non-
- 10 linearity, and the first subconverter stage gain is reduced to improve the conversion system bandwidth.